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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
LAM, NELSON C	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 02/28/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/724,949	AURACHER ET AL.	
	Examiner	Art Unit	
	Nelson Lam	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 December 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4-7,9,12,15-24 and 26-35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4-7,9,12,15-24 and 26-35* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/30/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Applicants' amendment to 10/724,949 has been examined. The specification has not been amended. Claims 1-2, 4, 6-7, 9, 12, 15, 26 and 28 are amended. Dependent claims 3, 8, 10-11, 13-14 and 25 are cancelled. Claims 1-2, 4-7, 9, 12, 15-24 and 26-35 are pending.

Applicants' Amendment is considered persuasive in part and the applicable rejections from the prior office action along with new ground of rejection are incorporated herein.

2. The following is a quotation of the **second** paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. **Claim 18 is rejected under 35 U.S.C. 112, second paragraph**, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As per claim 18, the term "circuit arrays" is undefined. Applicants' specification discloses many different types of specific circuits. Applicants must specify which of the named circuits Applicants intend to claim.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. **Claims 1-2, 4-7, 9, 12, 15-21 and 27-35 are rejected under 35 U.S.C. 102(e)** as being anticipated by Vasishta et al. (U.S. Patent No. 6,823,499).

As per **claim 1**, Vasishta discloses an integrated circuit comprising:

a die having a surface (Fig. 2A; col. 1, line 49-52; col. 3, line 65-66);

a first area of first circuit cells in said die configurable by user defined interconnections from above said surface (Abstract; Fig. 2A, #100, #110, #112; col. 2, line 51-54; col. 4, line 1-4; col. 6, line 1-5); and

a second area comprising a plurality of sub-circuit cells forming a module, wherein said sub-circuit cells includes (i) one or more non-reusable circuit cells coupled to a custom specific layer in a custom design having a predefined functionality (Abstract; col. 4, line 1-10; col. 4, line 22-40; where the hard macros are non-reusable circuit cells) and (ii) one or more reusable circuit cells coupled to said custom specific layer in said custom design when said predefined functionality of said module is not used (Abstract; col. 4, line 1-10; col. 4, line 22-40; where soft macros are reusable circuit cells).

As per **claim 2**, Vasishta discloses the integrated circuit of claim 1, wherein said and of said reusable circuit cell comprises at least one of a buffer circuit cell, an inverter circuit cell, a flip-flop circuit cell, a latch circuit cell, and an OR gate circuit cell (Fig. 3, #54; col. 5, line 21-24; where a logic element is a buffer cell, an inverter cell, a flip-flop, a latch, an OR gate).

As per **claim 4**, Vasishta discloses the integrated circuit of claim 1, wherein said reusable circuit cell comprise a plurality of different circuit cell types (Fig. 3, #54; col. 5, line 21-24).

As per **claim 5**, Vasishta discloses the integrated circuit of claim 1, wherein each of said first circuit cells comprises an input terminal at said surface and an output terminal at said surface (col. 3, line 53-57; col. 4, line 45-52).

As per **claim 6**, Vasishta discloses the integrated circuit of claim 29, wherein said reusable circuit cell comprises a first input terminal and a first output terminal (col. 3, line 53-57; col. 4, line 45-52).

As per **claim 7**, Vasishta discloses the integrated circuit of claim 6, wherein said first input terminal is coupled by said one or more interconnection layers to a stable voltage signal line (Fig. 3; Fig. 4; col. 5, line 34-48; col. 6, line 14-20; where a power grid or mesh is a voltage signal line).

As per **claim 9**, Vasishta discloses the integrated circuit of claim 7, wherein said stable voltage line is a power rail (col. 5, line 45-48).

As per **claim 12**, Vasishta discloses the integrated circuit of claim 1, wherein said reusable circuit cell is configured as a repeater cell in a routing connection across said second area when said reusable circuit cell is coupled to said custom specific layer (Fig. 3; col. 5, line 20-24, where gate is a repeater cell; col. 4, line 1-10; col. 4, line 22-40; where soft macros are reusable cells).

As per **claim 15**, Vasishta discloses an integrated circuit comprising:

a die having a surface (Fig. 2A; col. 49-52; col. 3, line 65-66);

a first general purpose area of said die comprising general purpose circuit elements configurable by user defined interconnections from above said surface (Abstract; Fig. 2A, #100, #110, #112; col. 2, line 51-54; col. 4, line 1-4; col. 6, line 1-5); and

a plurality of second standard circuit areas comprising standard sub-circuits having one or more reusable circuit cells more complicated than said general purpose circuit elements and configurable by user defined interconnections from above said surface (Fig. 3, #44, #46, #48, #50, #52, #54; col. 5, line 12-24; col. 4, line 1-10; col. 4, line 22-40; where the soft macros are reusable circuit cells);

wherein (i) said plurality of second standard circuit areas are distributed across said first general purpose area at multiple locations (Fig. 3, #54; col. 5, line 12-24) and (ii) said one or more reusable circuit cells provides functionality that is reusable at said multiple locations in said first general purpose area (Fig. 3, #54; col. 5, line 22-24; col. 4, line 1-10; col. 4, line 22-40; where the soft macros are reusable circuit cells).

As per **claim 16**, Vasishta discloses the integrated circuit of claim 15, wherein said plurality of second standard circuit areas are distributed in a substantially uniform pattern (Fig. 3, #54; col. 5, line 21-24; col. 4, line 53-58, where uniform pattern is interpreted as being an array).

As per **claim 17**, Vasishta discloses the integrated circuit of claim 15, wherein said plurality of second standard circuit areas are distributed according to a repeating pattern (Fig. 3, #54; col. 5, line 21-24; col. 4, line 53-58, where repeating pattern is interpreted as being an array).

As per **claim 18**, Vasishta discloses the integrated circuit of claim 15, wherein said plurality of second standard circuit areas comprise a plurality of circuit arrays (Fig. 3, #54; col. 5, line 21-24; col. 4, line 53-58).

As per **claim 19**, Vasishta discloses the integrated circuit of claim 15, wherein said general purpose circuit elements comprise logic circuits (Fig. 3, #54; col. 5, line 21-24).

As per **claim 20**, Vasishta discloses the integrated circuit of claim 15, wherein said general purpose circuit elements comprise one or more logic gates (Fig. 3, #54; col. 5, line 21-24).

As per **claim 21**, Vasishta discloses the integrated circuit of claim 15, wherein said standard sub-circuits comprise logic circuits (Fig. 3, #54; col. 5, line 21-24).

As per **claim 27**, Vasishta discloses the integrated circuit of claim 15, further comprising:

at least one layer of conductive interconnections formed on said surface (Fig. 2B; col. 5, line 1-11);

wherein (i) said general purpose circuit elements are coupled to said conductive interconnections in said at least one layer (Fig. 4; col. 6, line 12-17), and (ii) said standard sub-circuits are coupled to said conductive interconnections in said at least one layer (Fig. 4; col. 6, line 12-17; col. 6, line 24-29).

As per **claim 28**, Vasishta discloses a method for designing an integrated circuit element, comprising the steps of:

(a) providing a first area of said integrated circuit element comprising first circuit cells configurable by user defined interconnections above a surface of said integrated circuit element (Abstract; Fig. 2A, #100, #110, #112; col. 2, line 51-54; col. 4, line 1-4; col. 6, line 1-5); and

(b) providing a second area of said integrated circuit element comprising a plurality of sub-circuit cells forming a module, wherein said sub-circuit cells includes (i) one or more non-reusable circuit cells coupled to a custom specific layer in a custom design having a predefined functionality (Abstract; col. 4, line 1-10; col. 4, line 22-40; where the hard macros are non-reusable circuit cells) and (ii) one or more reusable circuit cells coupled to said custom specific layer in said custom design when said predefined functionality of said module is not used. (Abstract; Fig. 2A, #100, #102, # 104; col. 2, line 44-51; col. 4, line 1-6; Abstract; col. 4, line 1-10; col. 4, line 22-40; where soft macros are reusable circuit cells).

As per **claim 29**, Vasishta discloses the integrated circuit of claim 1, wherein said custom specific layer comprises one or more interconnection layers (Fig. 2A, #110, #112; col. 6, line 1-7).

As per **claim 30**, Vasishta discloses the integrated circuit of claim 6, wherein said one or more reusable circuit cells are coupled to said one or more interconnection layers with said first input terminal and said first output terminal (col. 3, line 53-57; col. 4, line 1-52; where soft macros are reusable circuit cells).

As per **claim 31**, Vasishta discloses the integrated circuit of claim 1, wherein said reusable circuit cell includes one or more buffers and one or more invertors to provide

functionality that is reusable (Fig. 1; col. 3, line 45-49; col. 5, line 22-23; where a buffer cell and an inverter cell are logic gates).

As per **claim 32**, Vasishta discloses the integrated circuit of claim 1, wherein said custom specific layer is positioned above a conductive layer having one or more power distribution lines (col. 4, line 22-31).

As per **claim 33**, Vasishta discloses the integrated circuit of claim 1, wherein said module includes one or more buffer stacks, multi-location memories, signal processor cores, general processor cores, mathematical processor cores, encoders, decoders, transmitters, receivers, communication circuits, analog circuits, and hybrid circuits (col. 4, line 38-52).

As per **claim 34**, Vasishta discloses the integrated circuit of claim 15, wherein said standard sub-circuit comprises one or more non-reusable circuit cells to form one or more modules with one or more reusable circuit cells (col. 4, line 1-10; col. 4, line 22-40).

As per **claim 35**, Vasishta discloses the integrated circuit of claim 34, further comprising:

a customer specific layer in a custom design coupled to (i) said one or more non-reusable circuit cells in a custom design for said modules with a predefined functionality (Abstract; Fig. 2A, #100, #102, #104; col. 2, line 41-51; col. 4, line 1-10) and (ii) said one or more reusable circuit cells in said custom design when said predefined functionality for said modules is not used (col. 2, line 44-51; col. 4, line 1-10).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. **Claims 22-24 and 26 are rejected under 35 U.S.C. 103(a)** as being unpatentable over Vasishta in view of Actel Introduction to Actel FPGA Architecture (Actel Application Note). Vasishta discloses all the limitations of claim 15 referred above. However, Vasishta does not explicitly disclose the use of a buffer array cell but discloses a single logic element, such as a gate (Vasishta: col. 5, line 22-23). Actel Application Note discloses all the limitations of claim 15 referred above and discloses a simple I/O module (Fig. 8) that is part of an I/O interface unit (Fig. 1). The I/O interface unit represents a buffer array cell that Vasishta does not disclose. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to include the buffer array cell used in Actel Application Note into the method of Vasishta since the method of Vasishta includes an I/O interface unit which would use the I/O buffer array cells detailed in the Actel Application Note (Vasishta: col. 5, line 16-20).

As per **claim 22**, Actel Application Note discloses the integrated circuit of claim 15, wherein said standard sub-circuits comprise a first buffer array circuit cell. (Fig. 1, Fig. 8). I/O buffers as shown by the various configuration illustrated in the Actel Application Note are by definition buffer array circuit cells.

As per **claim 23**, Actel Application Note discloses the integrated circuit of claim 22, wherein said first buffer array circuit cell comprises an array of buffer circuits, wherein (i) each buffer circuit comprises an input terminal and an output terminal (Fig. 8, Fig. 9), and (ii) adjacent buffer circuits are oppositely orientated (Fig. 8, Fig. 9).

As per **claim 24**, Actel Application Note discloses the integrated circuit of claim 22 wherein said standard sub-circuits further comprise a second buffer array circuit cell extending in a different physical direction from said first buffer array circuit cell (Fig. 1, where the I/O buffers are shown in both horizontal and vertical directions).

As per **claim 26**, Actel Application Note discloses the integrated circuit of claim 24, wherein said standard sub-circuits comprise at least one of an individual buffer (Fig. 8 illustrates an individual buffer), a logic gate different from said general purpose circuit elements, a multiplexer (Fig. 4 illustrates a multiplexer), and a flip flop (Fig. 6; Fig. 7; Fig. 9; Fig. 10, all illustrate a D-type flip flop).

Remarks

8. Applicants state that Vasishta concerns a method for designing application specific integrated circuit structure. However, the Vasishta reference also discloses a structure for designing application specific integrated circuits. Examiner has already identified and referenced explanatory cites reading on these limitations in the non-final office action. Applicants have incorporated the reusable and non-reusable circuit cells limitations into amended independent claims 1, 15 and 28. Therefore, the amended claims are rejected over the prior art of record.

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nelson Lam whose telephone number is 571 272-8318. The examiner can normally be reached on Monday-Friday at 9am - 5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571 272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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